

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2003-084687

(43)Date of publication of application : 19.03.2003

(51)Int.Cl.

G09F 9/30
G02F 1/13
G02F 1/1335
G02F 1/1343
G02F 1/1368
G09F 9/35
H01L 21/20
H01L 21/322
H01L 21/336
H01L 29/786
H05B 33/14

(21)Application number : 2002-148441

(71)Applicant : SEMICONDUCTOR ENERGY LAB CO LTD

(22)Date of filing : 22.05.2002

(72)Inventor : ISHIKAWA AKIRA

(30)Priority

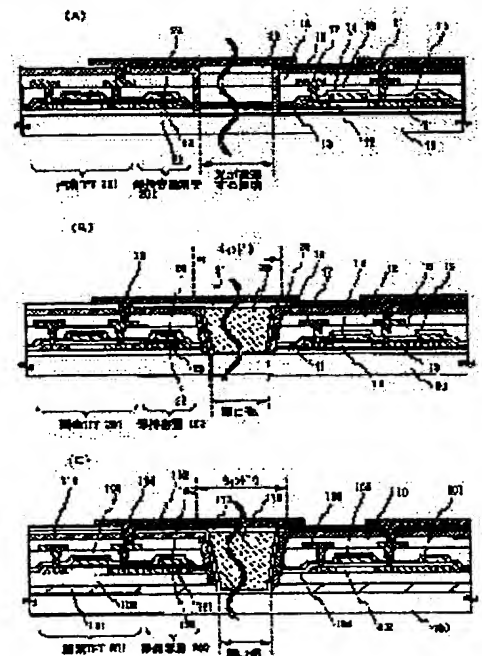
Priority number : 2001154673 Priority date : 23.05.2001 Priority country : JP

(54) SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method of realizing a semiconductor device having a structure capable of attaining the compatibility of a sufficient holding capacity with sufficient light shielding property without lowering the aperture ratio.

SOLUTION: A lower light shielding film is formed on a substrate and TFTs are formed on this lower light shielding film. An upper light shielding film is formed so as to cap the TFTs across an interlayer insulating film on the TFTs. As a result, the TFTs can be completely shielded from light by the upper light shielding film and the lower light shielding film and the generation of a light leakage current can be hindered.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted

[registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

* NOTICES *

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2. **** shows the word which can not be translated.

3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] In the semiconductor device which has an up light-shielding film between the pixel electrode electrically connected with TFT on a substrate, and said TFT, and said TFT and said pixel electrode It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. Said up light-shielding film is a semiconductor device characterized by being continuously formed on said interlayer insulation film so that said TFT may be inserted in from the base of said window, and forming opening in the interior of said window.

[Claim 2] In the semiconductor device which has an up light-shielding film between the lower light-shielding film on a substrate, the pixel electrode electrically connected with TFT and said TFT on said lower light-shielding film, and said TFT and said pixel electrode It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. It is the semiconductor device characterized by forming said up light-shielding film continuously on said interlayer insulation film so that said TFT may be inserted in from the base of said window, and the area of said window being almost equal to the area of opening.

[Claim 3] In the semiconductor device which has an up light-shielding film between the lower light-shielding film on a substrate, the pixel electrode electrically connected with TFT and said TFT on said lower light-shielding film, and said TFT and said pixel electrode It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. Said up light-shielding film is a semiconductor device which is continuously formed on said interlayer insulation film so that said TFT may be inserted in from the base of said window, and is characterized by said lower light-shielding film and said up light-shielding film having touched on the base of said window.

[Claim 4] The lower light-shielding film on a substrate, and the retention volume component formed with TFT on said lower light-shielding film at said TFT and juxtaposition, In the semiconductor device which has an up light-shielding film between the pixel electrode electrically connected with said TFT, and said TFT and said pixel electrode It is the semiconductor device which the interlayer insulation film of at least one layer is formed on said TFT and said retention volume component, has said window between said pixel electrodes and said substrates, and is characterized by said lower light-shielding film and said up light-shielding film having touched on the base of said window.

[Claim 5] In the semiconductor device which has a light-shielding film between the pixel electrode electrically connected with TFT on a substrate, and said TFT, and said TFT and said pixel electrode It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. It is the semiconductor device which flattening of said window is carried out by the translucency organic compound insulator, and is characterized by forming said light-shielding film continuously on said interlayer insulation film so that said TFT may be inserted in from the base of said window.

[Claim 6] The lower light-shielding film on a substrate, and the pixel electrode electrically connected with TFT and said TFT on said lower light-shielding film, In the semiconductor device with which two or more up light-shielding films and insulator layers have the layered product by which the laminating was carried out by turns

between said TFT(s) and said pixel electrodes It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. It is the semiconductor device which flattening of said window is carried out by the translucency organic compound insulator, and is characterized by forming said two or more up light-shielding films by which the laminating was carried out so that said TFT may be inserted in from the base of said window.

[Claim 7] The lower light-shielding film on a substrate, and the pixel electrode electrically connected with TFT and said TFT on said lower light-shielding film, In the semiconductor device which has the layered product by which the laminating of two or more up light-shielding films and insulator layers was carried out by turns between said TFT(s) and said pixel electrodes It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. Flattening of said window is carried out by the translucency organic compound insulator, and said two or more up light-shielding films by which the laminating was carried out are formed so that said TFT may be inserted in from the base of said window. The semiconductor device characterized by at least one up light-shielding film having connected said TFT and said pixel electrode electrically among said layered products.

[Claim 8] The lower light-shielding film on a substrate, and the pixel electrode electrically connected with TFT and said TFT on said lower light-shielding film, In the semiconductor device which has the layered product by which the laminating of two or more up light-shielding films and insulator layers was carried out by turns between said TFT(s) and said pixel electrodes It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. Flattening of said window is carried out by the translucency organic compound insulator, said two or more up light-shielding films by which the laminating was carried out are formed so that said TFT may be inserted in from the base of said window, and it sets to said layered product. The semiconductor device characterized by forming the retention volume component by said two or more up light-shielding films formed through said insulator layer and said insulator layer.

[Claim 9] In the semiconductor device which has the layered product by which the laminating of two or more up light-shielding films and insulator layers was carried out by turns between the pixel electrode electrically connected with TFT on a substrate, and said TFT, and said TFT and said pixel electrode It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and substrates, and was formed in it. Wiring which connects said TFT and said pixel electrode electrically the semiconductor device characterized by being almost equal to the field which meant that said up light-shielding film formed so that said TFT might be inserted in from the base of said window came out further, were, and the area of said window controlled a display in a pixel.

[Claim 10] The semiconductor device characterized by forming the lower light-shielding film between said substrate and said TFT in claim 9.

[Claim 11] The 1st layer of said up light-shielding film and said lower light-shielding film are a semiconductor device characterized by having touched [in / on claim 10 and / the base of said window between said pixel electrodes and substrates].

[Claim 12] It is the semiconductor device characterized by forming the photoresist film with which said window was colored R (red), G (green), and B (blue) in any 1 term of claim 1 thru/or claim 11, and the organic compound insulator of translucency.

[Claim 13] The process which forms a semi-conductor layer in an insulating front face, and the process which forms gate dielectric film on said semi-conductor layer, The process which forms a gate electrode on said gate dielectric film, and the process which forms the 1st interlayer insulation film on said gate electrode, The process which forms the process which forms the 2nd interlayer insulation film on said 1st interlayer insulation film, and the 1st contact hole which reaches said semi-conductor layer, and forms wiring for [each] connecting TFT electrically, The process which forms the slot which reaches a substrate between the process which forms the 3rd interlayer insulation film so that said wiring may be covered, and the field and TFT which light penetrates, The

process which forms a light-shielding film continuously from said 3rd interlayer insulation film to said slot, The process which forms the 2nd contact hole for connecting a pixel electrode and wiring, The production approach of the semiconductor device characterized by including the process which forms the 4th interlayer insulation film on said light-shielding film, the process which removes a part of insulator layer formed by said 2nd contact hole in order to expose said wiring, and the process which forms said pixel electrode.

[Claim 14] The process which forms a semi-conductor layer on an insulating front face, and the process which forms gate dielectric film on said semi-conductor layer, The process which forms a gate electrode on said gate dielectric film, and the process which forms the 1st interlayer insulation film on said gate electrode, The process which forms the process which forms the 2nd interlayer insulation film on said 1st interlayer insulation film, and the 1st contact hole which reaches said semi-conductor layer, and forms wiring for [each] connecting TFT electrically, The process which forms the window which removes the substrate insulator layer of the process which forms the 3rd interlayer insulation film so that said wiring may be covered, and the field which light penetrates, gate dielectric film, the 1st interlayer insulation film, and the 2nd interlayer insulation film, and reaches a substrate, The process which forms an up light-shielding film so that TFT may be inserted in on said 3rd interlayer insulation film, The process which removes said lower light-shielding film formed in said window base, The process which forms the 2nd contact hole in said up light-shielding film, and the process which forms the 4th interlayer insulation film on said up light-shielding film, The process which carries out flattening of said window by the insulator layer which has light transmission nature, The production approach of the semiconductor device characterized by including the process which forms the 5th interlayer insulation film on said up light-shielding film, the process which removes a part of insulator layer buried with said 2nd contact hole so that said wiring might be exposed, and the process which forms a pixel electrode on said 5th interlayer insulation film.

[Claim 15] The process which forms a semi-conductor layer on an insulating front face, and the process which forms gate dielectric film on said semi-conductor layer, The process which forms a gate electrode on said gate dielectric film, and the process which forms the 1st interlayer insulation film on said gate electrode, The process which forms the process which forms the 2nd interlayer insulation film on said 1st interlayer insulation film, and the 1st contact hole which reaches said semi-conductor layer, and forms wiring for [each] connecting TFT electrically, The process which forms the window which removes the substrate insulator layer of the process which forms the 3rd interlayer insulation film so that said wiring may be covered, and the field which light penetrates, gate dielectric film, the 1st interlayer insulation film, and the 2nd interlayer insulation film, and reaches a substrate, The process which forms the 1st light-shielding film of the upper part so that TFT may be inserted in on said 3rd interlayer insulation film, The process which forms in said 1st light-shielding film of the upper part and said 3rd interlayer insulation film the 2nd contact hole which reaches said wiring, The process which forms the 1st insulator layer on said 1st light-shielding film of the upper part, and the process which removes said a part of 1st insulator layer buried with said 2nd contact hole so that said wiring might be exposed, The process which forms the 2nd light-shielding film of the upper part on said 1st insulator layer, and the process which forms the 2nd insulator layer on said 2nd light-shielding film of the upper part, The process which removes the process which forms the 3rd light-shielding film of the upper part on said 2nd insulator layer, the lower light-shielding film formed in said window base, said 1st light-shielding film of the upper part, said 1st insulator layer, said 2nd light-shielding film of the upper part, said 2nd insulator layer, and said 3rd light-shielding film of the upper part, The process which forms in said 3rd light-shielding film of the upper part and said 2nd insulator layer the 3rd contact hole which reaches said 2nd light-shielding film of the upper part, The process which forms the 4th interlayer insulation film, and the process which carries out flattening of said window by the insulator layer which has light transmission nature, The process which forms the 5th interlayer insulation film on said 3rd light-shielding film of the upper part, and the process which removes a part of insulator layer buried with said 3rd contact hole so that said 2nd light-shielding film of the upper part might be exposed, The production approach of the semiconductor device characterized by including the process which forms a pixel electrode on said 5th interlayer insulation film.

[Claim 16] The production approach of the semiconductor device characterized by including the process which forms a lower light-shielding film on an insulating front face in any 1 term of claim 13 thru/or claim 15.

[Claim 17] It is the production approach of the semiconductor device characterized by connecting wiring with which said lower light-shielding film, said 1st up light-shielding film, and said 3rd up light-shielding film serve as touch-down potential in any 1 term of claim 13 thru/or claim 15.

[Claim 18] It is the production approach of the semiconductor device characterized by forming so that said lower light-shielding film and said up light-shielding film may touch on the base of said window in claim 14.

[Claim 19] The process which carries out flattening of said window in any 1 term of claim 14 thru/or claim 18 is the production approach of the semiconductor device characterized by carrying out using an organic compound insulator.

[Claim 20] The process which carries out flattening of said window in any 1 term of claim 14 thru/or claim 19 is the production approach of the semiconductor device characterized by carrying out the laminating of the photoresist film colored R (red), G (green), or B (blue) and the transparence organic compound insulator, and performing them.

[Claim 21] It is the production approach of the semiconductor device characterized by crystallizing when said semi-conductor layer irradiates a laser beam in any 1 term of claim 13 thru/or claim 20.

[Claim 22] It is the production approach of the semiconductor device which carries out gettering of said catalyst element, and is characterized by being the crystalline substance semi-conductor film which is made to reduce the catalyst element concentration in a semi-conductor layer, and is obtained after crystallizing said semi-conductor layer in any 1 term of claim 13 thru/or claim 21 using a catalyst element.

[Translation done.]

*** NOTICES ***

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a thin film transistor (Thin Film Transistor:TFT) at the semiconductor device and representation target which used especially the crystalline substance semi-conductor film for the semi-conductor layer including a channel formation field, a source field, and a drain field. Moreover, it is related with the semiconductor device (especially related with a liquid crystal display and luminescence equipment) which used such TFT for the switching element of a drive circuit or a pixel, and its production technique. Moreover, it is related with the semiconductor device which has the structure which raised protection-from-light nature especially, and its production technique.

[0002]

[Description of the Prior Art] In recent years, the liquid crystal projector which employed the small lightweight description efficiently has come to be used in various scenes. Development competition for offering a still smaller and lightweight liquid crystal projector is violently performed so that it may unite with it. These liquid crystal projectors have composition which projects the image displayed on the liquid crystal display, and the display quality of a liquid crystal display influences the engine performance of a liquid crystal projector greatly.

[0003] As for a liquid crystal display, what encloses liquid crystal between the substrate (henceforth a TFT

substrate) with which TFT and a pixel electrode were formed, and the substrate (henceforth an opposite substrate) with which the counterelectrode was formed, and controls and carries out image display of the orientation of liquid crystal by the electric field between a pixel electrode and a counterelectrode is in use.

[0004] As a liquid crystal display, the active matrix liquid crystal display (liquid crystal panel) which has millions of pixels is briskly used for the pixel section in recent years. TFT is prepared in each pixel as a switching element to which such a liquid crystal panel impresses potential to each pixel, a pixel electrode is prepared in each TFT, the potential of a pixel electrode is set up at the time of on, and TFT holds the potential of a pixel electrode with the charge with which TFT was stored in the retention volume component (henceforth retention volume) at the time of off.

[0005] It is required that TFT should fully be large compared with the amount of charges in which the amount of charges accumulated in controlling the leakage current of TFT to the TFT substrate of a active-matrix mold since display quality will deteriorate if the potential of a pixel electrode is changed in between at the time of off, fully taking the retention volume for every pixel, and retention volume is lost according to leakage current.

[0006] Moreover, the field which meant controlling a display in opening, i.e., a pixel, in order to raise brightness in the case of a transparency mold liquid crystal panel (for example, it sets to the display of a transparency mold) In the display of the field and reflective mold which light penetrates and are contributed to a display, it is required with the field which light is reflected and contributes to a display, and the display using an organic light emitting device that the rate that the field which the organic luminous layer inserted into the electrode emits light, and contributes to a display occupies should be raised.

[0007] By the way, in order for the leakage current (henceforth optical leakage current) resulting from optical pumping to occur and to have a bad influence on a display if light carries out incidence to the semi-conductor layer of TFT when using for a liquid crystal projector a liquid crystal panel (especially transparency mold liquid crystal panel) which was described above, the protection-from-light layer is prepared in the liquid crystal panel. For example, when the light source of a projector has been arranged to the opposite substrate side, a protection-from-light layer is formed between a pixel electrode and TFT, the light from the light source is shaded or the light which formed the protection-from-light layer between the substrate and the semi-conductor layer, and was reflected in it with the projection lens etc. is shaded. Moreover, in the JP,2000-164875,A official report, a crevice is established in a substrate and a lower light-shielding film is formed all over a crevice internal surface, and it is formed so that the channel formation field of TFT may lay underground in this crevice. Moreover, the up light-shielding film is also formed collectively.

[0008] However, since irregularity is made near the TFT which various wiring concentrates with the structure indicated in the above-mentioned official report, possibility which is easy to produce a wiring short circuit and an open circuit in wiring formation of lowering the yield, such as electric-field concentration taking place and being easy to deteriorate, is high.

[0009] Moreover, with the structure indicated in the above-mentioned official report, a clearance is between an up light-shielding film and a lower light-shielding film, and the optical leakage current by the stray light may arise in such structure. Furthermore, in order to establish a crevice in a substrate, the mechanical strength of a substrate may become weak.

[0010]

[Problem(s) to be Solved by the Invention] Highly minute-ization is achieved by increasing the number of pixels of the panel which high brightness and the projector with which highly minute-ization is demanded raise display brightness by raising the reinforcement of the lamp first used for the light source, and get down utterly, and is used for optical system. However, a light-shielding film is formed between the conventional pixel electrode and TFT, or the light diffracted at the light-shielding film edge carries out incidence of the approach which has formed the light-shielding film enough and carries out it between a substrate and a semi-conductor layer to a semi-conductor layer, and there is a problem that optical leakage current will occur. Furthermore, high brightness-ization of the light source progresses and the bad influence to TFT by this diffracted light is being set to the level which cannot be disregarded.

[0011] Moreover, although it can decrease even to extent which can disregard the diffracted-light reinforcement in the location of TFT by thin-film-izing the insulator layer which separates a light-shielding film and TFT, thin film-ization of an insulator layer increases the parasitic capacitance generated between TFT and an insulator layer, and the problem that the potential of a light-shielding film will influence actuation of TFT generates it.

[0012] Moreover, although it is solvable about the problem in which the diffracted light carries out incidence to TFT by expanding the width of face of a light-shielding film, naturally the decline in a numerical aperture cannot be denied. And since it corresponds by making the number of pixels increase to the demand to highly-minute-izing of a display, each pixel size is reduced and the fall of the brightness accompanying decline in the numerical aperture by expanding the width of face of a light-shielding film and it poses a big problem.

[0013] Moreover, the stray light by dispersion which is not meant in an interlayer insulation film cannot solve the problem which carries out incidence to TFT (especially semi-conductor layer) only by expanding the width of face of a light-shielding film. The effect of the stray light cannot be disregarded in connection with the high brightness of the light source which was described above, either.

[0014] Moreover, there is an inclination for optical leakage current to become large compared with TFT containing an amorphous semiconductor layer, the charges stored when it did not have sufficient retention volume decrease in number for leakage current, the amount of transmitted lights changes, and TFT containing the barrier layer which has the crystal structure which has come to be positively used from the height of electric field effect mobility etc. causes [of image display] a contrast fall. Therefore, it is necessary to form the retention volume component which can secure sufficient capacity for a liquid crystal panel.

[0015] However, if it is going to extend the area of retention volume superficially in order to secure sufficient capacity, the rate that a retention volume component occupies in the area of a pixel will become large, and a numerical aperture will fall.

[0016] Furthermore, in order to raise the yield, it is necessary to consider as structure which an open circuit of wiring etc. does not produce with the irregularity by retention volume.

[0017] So, let it be a technical problem to offer the approach of realizing the semiconductor device which has the structure it can be [structure] compatible in sufficient protection-from-light nature and sufficient retention volume in this invention, without lowering a numerical aperture in view of the above problems.

[0018]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, this invention person considered the structure of reducing the diffracted light which carries out incidence to the semi-conductor layer of TFT, and the stray light, by forming a light-shielding film so that TFT may be inserted in.

[0019] An example of the structure of the pixel which adopted this invention is shown in drawing 1 (A). A light-shielding film is formed between a pixel electrode and TFT. In this specification, the light-shielding film by which at least the part was formed between a pixel electrode and TFT is called up light-shielding film. Light penetrates in a pixel, a slot is formed between the fields and TFT(s) which control a display, and the electric conduction film used as an up light-shielding film is formed. Conventionally, it is the structure where the up light-shielding film was continuously formed to the field which light penetrates from between a pixel electrode and TFT(s) unlike the light-shielding film currently formed between TFT and a pixel electrode, and TFT was inserted in by the up insulator layer.

[0020] Other structures of TFT which adopted other invention are shown in drawing 1 (B). After forming TFT which consists of a semi-conductor layer, gate dielectric film, and a gate electrode and forming an interlayer insulation film, light penetrates behind and the gate dielectric film of the field which controls a display, and its boundary region, and an interlayer insulation film are removed. In this specification, it is the hole-like field (it has the wall surface and the base) where some of gate dielectric film and interlayer insulation films were removed, and since it is easy, suppose that the field (opening) which meant controlling a display in a display, and the field which has the almost same area are called a hole or a window. Although the up light-shielding film and the insulator layer are formed and the area of opening becomes narrow from the area of a part for the thickness, and a window, if it becomes the area of a window, and the area of opening with the same area substantially, it can say to the

wall surface of a window.

[0021] In the window of drawing 1 (B), as compared with the slot on drawing 1 (A), since the aspect ratio of a window is small, its formation of an up light-shielding film is simple here. Subsequently, a light-shielding film is continuously formed so that the side face of a window may be covered for a light-shielding film from on TFT. And after removing the light-shielding film formed in the base (field which especially light penetrates) of a window, an insulator layer is formed and flattening of a window is performed using transparent organic resin film, such as an acrylic. Subsequently, an insulator layer is formed so that a light-shielding film and a pixel electrode may not contact, and a pixel electrode is formed further. It is the structure which TFT was inserted in by the up light-shielding film, and removed the interlayer insulation film, formed the window, and carried out flattening by the organic resin insulator layer of translucency.

[0022] In the case of the above structures, the area of the field (window) where some of these gate dielectric film and interlayer insulation films were removed is an area almost equal to the field (opening) which meant controlling a display in a pixel, and the field (opening) which meant controlling a display serves as an area narrower than said field (window) where some of gate dielectric film and interlayer insulation films were removed at least.

[0023] Other structures of the pixel which adopted other invention are shown in drawing 1 (C). In the example shown in drawing 1 (C), in order that the light which carries out incidence from a substrate side may also shade, before forming a semi-conductor layer, a light-shielding film is formed between a substrate and a semi-conductor layer. In addition, this light-shielding film formed between a substrate and a semi-conductor layer is hereafter called lower light-shielding film in this specification. Subsequently, after forming TFT which consists of a semi-conductor layer, gate dielectric film, and a gate electrode and forming an interlayer insulation film, the gate dielectric film and the interlayer insulation film which were formed in the field which controls a display, the becoming field, and its boundary region are removed behind, and a window is formed in it. Subsequently, a light-shielding film is continuously formed for a light-shielding film from TFT to a window. And the lower light-shielding film and up light-shielding film which are formed in the base of a window are removed, and opening (field which meant controlling a display) is formed. Subsequently, an insulator layer is formed and flattening of a window is performed using transparent organic resin film, such as an acrylic. Subsequently, a pixel electrode is formed, after forming an insulator layer so that a light-shielding film and a pixel electrode may not contact. It is the structure where TFT was inserted in by the up light-shielding film and was completely shaded by the lower light-shielding film and the up light-shielding film. In addition, it is also possible to cover touch-down potential, then TFT for a lower light-shielding film and an up light-shielding film electrically.

[0024] Furthermore, when it was going to form the color filter in the opposite substrate side, there was a problem that the precision which adjusts a TFT substrate and an opposite substrate will become severe by the fall of the pixel size accompanying highly-minute-izing. Then, although how to form a color filter in a TFT substrate side is considered, a pixel electrode must be formed after forming a color filter for carrying out orientation of the liquid crystal. However, the thickness of 1 micrometers or more was required for the color filter, and it was difficult to have made it flow through the pixel electrode separated by the color filter and a drain electrode.

[0025] Then, in the example shown in drawing 1 (B) and drawing 1 (C), the same function as the color filter currently formed in the opposite substrate comes to be obtained by performing flattening of a window using the photoresist film colored by R (red), G (green), or B (blue).

[0026] Moreover, although not illustrated, if an up light-shielding film is constituted from an ingredient with high reflection factors, such as aluminum, and the up light-shielding film of the base of the field (window) where some of gate dielectric film and interlayer insulation films were removed at least is not removed in the structure of drawing 1 (B) and (C) but it uses as a reflecting plate, considering as the display of a reflective mold is also possible.

[0027] In the semiconductor device which has a light-shielding film between the pixel electrode by which this invention is electrically connected with TFT on a substrate, and said TFT, and said TFT and said pixel electrode It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. Said light-

shielding film is continuously formed on said interlayer insulation film so that said TFT may be inserted in from the base of said window, and area of said window is characterized by being almost equal to the area of opening.

[0028] Moreover, this invention is set to the semiconductor device which has an up light-shielding film between the lower light-shielding film on a substrate, the pixel electrode electrically connected with TFT and said TFT on said lower light-shielding film, and said TFT and said pixel electrode. It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. Said up light-shielding film is continuously formed on said interlayer insulation film so that said TFT may be inserted in from the base of said window, and area of said window is characterized by being almost equal to the area of opening.

[0029] Moreover, this invention is set to the semiconductor device which has an up light-shielding film between the lower light-shielding film on a substrate, the pixel electrode electrically connected with TFT and said TFT on said lower light-shielding film, and said TFT and said pixel electrode. It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. Said up light-shielding film is continuously formed on said interlayer insulation film so that said TFT may be inserted in from the base of said window, and said lower light-shielding film and said up light-shielding film are characterized by having touched on the base of said window.

[0030] This invention on the lower light-shielding film on a substrate, and said lower light-shielding film Moreover, TFT, In the semiconductor device which has an up light-shielding film between the retention volume component formed in said TFT and juxtaposition, the pixel electrode electrically connected with said TFT, and said TFT and said pixel electrode On said TFT and said retention volume component, the interlayer insulation film of at least one layer is formed. It has the window which removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it, and said lower light-shielding film and said up light-shielding film are characterized by having touched on the base of said window.

[0031] Moreover, this invention is set to the semiconductor device which has a light-shielding film between the pixel electrode electrically connected with TFT on a substrate, and said TFT, and said TFT and said pixel electrode. It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. Flattening of said window is carried out by the translucency organic compound insulator, and it is characterized by forming said light-shielding film continuously on said interlayer insulation film so that said TFT may be inserted in from the base of said window.

[0032] This invention on the lower light-shielding film on a substrate, and said lower light-shielding film Moreover, TFT, In the semiconductor device with which two or more up light-shielding films and insulator layers have the layered product by which the laminating was carried out by turns between the pixel electrode electrically connected with said TFT, and said TFT and said pixel electrode It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. Flattening of said window is carried out by the translucency organic compound insulator, and it is characterized by forming said two or more up light-shielding films by which the laminating was carried out so that said TFT may be inserted in from the base of said window.

[0033] This invention on the lower light-shielding film on a substrate, and said lower light-shielding film Moreover, TFT, In the semiconductor device which has the layered product by which the laminating of two or more up light-shielding films and insulator layers was carried out by turns between the pixel electrode electrically connected with said TFT, and said TFT and said pixel electrode It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and said substrates, and was formed in it. Flattening of said window is carried out by the translucency organic compound insulator, and said two or more up light-shielding films by which the laminating was carried out are formed so that said TFT may be inserted in from the base of said window. It is characterized by at least one up light-shielding film having connected said TFT and said pixel electrode electrically among said layered products.

[0034] This invention on the lower light-shielding film on a substrate, and said lower light-shielding film Moreover,

TFT, In the semiconductor device which has the layered product by which the laminating of two or more up light-shielding films and insulator layers was carried out by turns between the pixel electrode electrically connected with said TFT, and said TFT and said pixel electrode It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film and was formed between said pixel electrodes and said radicals. Flattening of said window is carried out by the translucency organic compound insulator, said two or more up light-shielding films by which the laminating was carried out are formed so that said TFT may be inserted in from the base of said window, and it sets to said layered product. It is characterized by forming the retention volume component by said two or more up light-shielding films formed through said insulator layer and said insulator layer.

[0035] Moreover, this invention is set to the semiconductor device which has the layered product by which the laminating of two or more up light-shielding films and insulator layers was carried out by turns between the pixel electrode electrically connected with TFT on a substrate, and said TFT, and said TFT and said pixel electrode. It has the window which the interlayer insulation film of at least one layer was formed on said TFT, and removed said interlayer insulation film between said pixel electrodes and substrates, and was formed in it. said up light-shielding film formed so that said TFT might be inserted in from the base of said window comes out further, there is wiring which connects said TFT and said pixel electrode electrically, and area of said window is characterized by being almost equal to the field which meant controlling a display in a pixel.

[0036] Moreover, in the above-mentioned invention, it is characterized by forming the lower light-shielding film between said substrate and said TFT.

[0037] Moreover, in the above-mentioned invention, the 1st layer of said up light-shielding film and said lower light-shielding film are characterized by having touched in the base of said window between said pixel electrodes and substrates.

[0038] Moreover, in the above-mentioned invention, said window is characterized by forming the photoresist film colored R (red), G (green), and B (blue) and the organic compound insulator of translucency.

[0039] Moreover, the process at which this invention forms a semi-conductor layer in an insulating front face and the process which forms gate dielectric film on said semi-conductor layer, The process which forms a gate electrode on said gate dielectric film, and the process which forms the 1st interlayer insulation film on said gate electrode, The process which forms the process which forms the 2nd interlayer insulation film on said 1st interlayer insulation film, and the 1st contact hole which reaches said semi-conductor layer, and forms wiring for [each] connecting TFT electrically, The process which forms the slot which reaches a substrate between the process which forms the 3rd interlayer insulation film so that said wiring may be covered, and the field and TFT which light penetrates, The process which forms a light-shielding film continuously from said 3rd interlayer insulation film to said slot, The process which forms the 2nd contact hole for connecting a pixel electrode and wiring, It is characterized by including the process which forms the 4th interlayer insulation film on said light-shielding film, the process which removes a part of insulator layer formed by said 2nd contact hole in order to expose said wiring, and the process which forms said pixel electrode.

[0040] Moreover, the process at which this invention forms a semi-conductor layer on an insulating front face and the process which forms gate dielectric film on said semi-conductor layer, The process which forms a gate electrode on said gate dielectric film, and the process which forms the 1st interlayer insulation film on said gate electrode, The process which forms the process which forms the 2nd interlayer insulation film on said 1st interlayer insulation film, and the 1st contact hole which reaches said semi-conductor layer, and forms wiring for [each] connecting TFT electrically, The process which forms the window which removes the substrate insulator layer of the process which forms the 3rd interlayer insulation film so that said wiring may be covered, and the field which light penetrates, gate dielectric film, the 1st interlayer insulation film, and the 2nd interlayer insulation film, and reaches a substrate, The process which forms an up light-shielding film so that TFT may be inserted in on said 3rd interlayer insulation film, By the process which removes the lower light-shielding film formed in said window base, the process which forms the 2nd contact hole in said up light-shielding film, the process which forms the 4th interlayer insulation film on said up light-shielding film, and the insulator layer which has light

transmission nature The process which carries out flattening of said window, and the process which forms the 5th interlayer insulation film on said up light-shielding film, It is characterized by including the process which removes a part of insulator layer buried with said 2nd contact hole so that said wiring might be exposed, and the process which forms a pixel electrode on said 5th interlayer insulation film.

[0041] Moreover, the process at which this invention forms a semi-conductor layer on an insulating front face and the process which forms gate dielectric film on said semi-conductor layer, The process which forms a gate electrode on said gate dielectric film, and the process which forms the 1st interlayer insulation film on said gate electrode, The process which forms the process which forms the 2nd interlayer insulation film on said 1st interlayer insulation film, and the 1st contact hole which reaches said semi-conductor layer, and forms wiring for [each] connecting TFT electrically, The process which forms the window which removes the substrate insulator layer of the process which forms the 3rd interlayer insulation film so that said wiring may be covered, and the field which light penetrates, gate dielectric film, the 1st interlayer insulation film, and the 2nd interlayer insulation film, and reaches a substrate, The process which forms the 1st light-shielding film of the upper part so that TFT may be inserted in on said 3rd interlayer insulation film, The process which forms in said 1st light-shielding film of the upper part and said 3rd interlayer insulation film the 2nd contact hole which reaches said wiring, The process which forms the 1st insulator layer on said 1st light-shielding film of the upper part, and the process which removes said a part of 1st insulator layer buried with said 2nd contact hole so that said wiring might be exposed, The process which forms the 2nd light-shielding film of the upper part on said 1st insulator layer, and the process which forms the 2nd insulator layer on said 2nd light-shielding film of the upper part, The process which removes the process which forms the 3rd light-shielding film of the upper part on said 2nd insulator layer, the lower light-shielding film formed in said window base, said 1st light-shielding film of the upper part, said 1st insulator layer, said 2nd light-shielding film of the upper part, said 2nd insulator layer, and said 3rd light-shielding film of the upper part, The process which forms in said 3rd light-shielding film of the upper part and said 2nd insulator layer the 3rd contact hole which reaches said 2nd light-shielding film of the upper part, The process which forms the 4th interlayer insulation film, and the process which carries out flattening of said window by the insulator layer which has light transmission nature, It is characterized by including the process which forms the 5th interlayer insulation film on said 3rd light-shielding film of the upper part, the process which removes a part of insulator layer buried with said 3rd contact hole so that said 2nd light-shielding film of the upper part might be exposed, and the process which forms a pixel electrode on said 5th interlayer insulation film.

[0042] Moreover, in the above-mentioned invention, it is characterized by including the process which forms a lower light-shielding film on an insulating front face.

[0043] Moreover, in the above-mentioned invention, said lower light-shielding film, said 1st up light-shielding film, and said 3rd up light-shielding film are characterized by connecting wiring which serves as touch-down potential.

[0044] Moreover, in the above-mentioned invention, said lower light-shielding film and said up light-shielding film are characterized by forming so that it may touch on the base of said window.

[0045] Moreover, in the above-mentioned invention, the process which carries out flattening of said said window is characterized by carrying out using an organic compound insulator.

[0046] Moreover, in the above-mentioned invention, the process which carries out flattening of said said window is characterized by carrying out the laminating of the photoresist film colored R (red), G (green), or B (blue) and the transparence organic compound insulator, and performing them.

[0047] Moreover, in the above-mentioned invention, said semi-conductor layer is characterized by crystallizing by irradiating a laser beam.

[0048] Moreover, in the above-mentioned invention, after crystallizing using a catalyst element, said semi-conductor layer carries out gettering of said catalyst element, and is characterized by being the crystalline substance semi-conductor film which is made to reduce the catalyst element concentration in a semi-conductor layer, and is obtained.

[0049] As mentioned above, this invention makes TFT wrap structure by the light-shielding film, in order to prevent the optical leakage current generated by the light which means and carries out the diffracted light, the

stray light, etc., and carries out incidence to the semi-conductor layer of TFT.

[0050]

[Embodiment of the Invention] (Operation gestalt 1) The structure of the transparency mold liquid crystal display produced using this invention using drawing 1 (A) is explained.

[0051] The substrate insulator layer 11 is formed on the substrate 10, and TFT which consists of the semi-conductor layer 12, gate dielectric film 13, and a gate electrode 14 is formed on the substrate insulator layer 11. On the gate electrode 14, the 1st interlayer insulation film 15 and the 2nd interlayer insulation film 16 are formed. Flattening of the 2nd interlayer insulation film 16 is carried out if needed. Then, each wiring 17 which connects TFT electrically is connected and formed in the source field or drain field of the semi-conductor layer 12. A slot is formed in the boundary line of TFT and opening, after covering wiring 17 and forming the 3rd interlayer insulation film 18. A slot is formed so that a substrate may be reached. Subsequently, the electric conduction film is continuously formed into a slot from on the 3rd interlayer insulation film 18 with a metal CVD method, and a light-shielding film 19 is formed. Then, after forming the 4th interlayer insulation film 20, the pixel electrode 21 is formed so that a light-shielding film 19 may not be touched.

[0052] In addition, retention volume 202 is formed with the insulator layer 23 (dielectric) of the same layer as the field 22 (one electrode of retention volume) and gate dielectric film 13 which continued from the semi-conductor layer 12, and the capacity wiring 24 (another electrode of retention volume) of the same layer as the gate electrode 14.

[0053] In the field which the semiconductor device of this invention has TFT201 covered with the light-shielding film 19 continuously formed from between TFT201 and pixel electrodes to the boundary line of TFT201 and opening (field which meant controlling a display) in each pixel of the pixel section, and the light of a pixel penetrates It is the structure where the laminating of the substrate insulator layer 11, gate dielectric film 13, the 1st interlayer insulation film 15, the 2nd interlayer insulation film 16, the 3rd interlayer insulation film 18, and the 4th interlayer insulation film 20 is carried out between the pixel electrode and the substrate.

[0054] Moreover, in TFT of the structure shown in drawing 1 (A), it is good also as structure which prepared the light-shielding film (lower light-shielding film) between the substrate 10 and the semi-conductor layer 12. In this case, the depth of flute with which a light-shielding film is filled up may be the depth which does not arrive that an operation person should just determine suitably even if it is the depth which reaches a lower light-shielding film.

[0055] (Operation gestalt 2) Other structures of TFT of this invention are explained using drawing 1 (B). In addition, when you point out the same thing as drawing 1 (A), suppose that the same sign is used.

[0056] The substrate insulator layer 11 is formed on the substrate 10, and TFT which consists of the semi-conductor layer 12, gate dielectric film 13, and a gate electrode 14 is formed on the substrate insulator layer 11. On the gate electrode 14, the 1st interlayer insulation film 15 and the 2nd interlayer insulation film 16 are formed. Flattening of the 2nd interlayer insulation film 16 is carried out if needed. Then, each wiring 17 which connects TFT electrically is connected and formed in the source field or drain field of the semi-conductor layer 12. After covering wiring 17 and forming the 3rd interlayer insulation film 18, the 3rd interlayer insulation film 18, the 2nd interlayer insulation film 16, the 1st interlayer insulation film 15, the gate dielectric film 13, and the substrate insulator layer 11 of the range a little larger than opening (field which meant controlling a display) are removed. Subsequently, the electric conduction film is continuously formed along the side face of a field (window) in which gate dielectric film and an interlayer insulation film were removed from on the 3rd interlayer insulation film 18, and the up light-shielding film 19 is formed. Subsequently, the up light-shielding film 19 formed in the window base is removed, and the 4th interlayer insulation film 20 is formed. Then, the organic compound insulator of light transmission nature etc. carries out flattening of the window by 30, the 5th interlayer insulation film 31 is formed on it, and the pixel electrode 32 is formed.

[0057] TFT of this invention is formed so that a light-shielding film may insert in TFT from the field (window) base where some of gate dielectric film and interlayer insulation films were removed at least, and there is opening in the interior of a window. In this example, since the aspect ratio of a window is small, even if production of the up

light-shielding film 19 uses a spatter simpler than a metal CVD method, it can obtain good coverage.

[0058] Moreover, since TFT can be covered by the light-shielding film, generating of optical leakage current can be suppressed.

[0059] (Operation gestalt 3) Other structures of TFT of this invention are explained using drawing 1 (C).

[0060] The lower light-shielding film 101 is formed on the substrate 100, and it is formed on the lower light-shielding film 101 in order of the substrate insulator layer 102, the semi-conductor layer 103, and gate dielectric film 104. On gate dielectric film 104, 108 ****s of the 1st interlayer insulation film 107 and 2nd interlayer insulation film are carried out on the gate electrode 105 and the gate electrode 105, on the 2nd interlayer insulation film, the wiring 109 which connected with the source field or drain field of the semi-conductor layer 103 is formed, wiring 109 is covered and the 3rd interlayer insulation film 110 is formed. Moreover, the up light-shielding film 111 is formed on the 3rd interlayer insulation film 110.

[0061] Moreover, on the up light-shielding film 111, the pixel electrode 114 is formed through the insulator layer 112. The pixel electrode 114 is connected to wiring connected to the drain field of TFT through the contact hole formed in the up light-shielding film 111 and the 3rd interlayer insulation film 110. Moreover, retention volume 202 consists of the semi-conductor layer 120, an insulator layer 121, and capacity wiring 106. The semi-conductor layer 120 is continuously formed from the drain field, and it has become one electrode of retention volume. The insulator layer 121 of the same layer as gate dielectric film serves as a dielectric of retention volume, and the capacity wiring 106 formed in the same layer as a gate electrode serves as another electrode of retention volume.

[0062] Such TFT201 and retention volume 202 are formed in each pixel. In addition, opening is formed in the interior of the window where the 3rd interlayer insulation film 110, the 2nd interlayer insulation film 108, the 1st interlayer insulation film 107, gate dielectric film 104, and the lower light-shielding film 101 were removed. Moreover, the up light-shielding film is formed from on the 2nd interlayer insulation film 108 succeeding the window wall surface. However, the up light-shielding film formed in the window base is removed.

[0063] It is touched and formed at the pars basilaris ossis occipitalis of a window so that it may become the touch-down potential with same lower light-shielding film 101 and up light-shielding film 111, and although not illustrated, it connects with wiring which gives touch-down potential.

[0064] In addition, flattening of the window is carried out using the organic compound insulators 115, such as an acrylic. Moreover, after carrying out flattening, the pixel electrode 114 is formed. The pixel electrode 114 takes wiring and the flow which were connected to the drain field of the semi-conductor layer 103, and TFT201 and the pixel electrode 114 are connected electrically.

[0065] As mentioned above, it is formed so that the up light-shielding film 111 may insert in TFT of the pixel section, and the liquid crystal panel completely shaded by the lower light-shielding film 101 and the up light-shielding film 111 can be produced.

[0066]

[Example] (Example 1) In this example, the process which produces a active-matrix substrate using this invention is explained.

[0067] First, in order to form the lower light-shielding film 301 on the quartz substrate 300, the laminating of the polish recon film and the WSix film is carried out, and they are formed. In addition, its thermal resistance which has the protection-from-light nature which fulfills a demand level, and can be equal to the heat-treatment for activation of TFT is indispensable, and since considering as touch-down potential further is desirable as for the lower light-shielding film 301, it is desirable [the light-shielding film] that it is the electric conduction film. Then, one which consists of conductive ingredients, such as polish recon film, WSix ($x=2.0-2.8$) film, and aluminum, Ta, W, Cr, Mo, of film kinds, or two or more sorts should just be used for the film used as a lower light-shielding film (drawing 2 (A)).

[0068] Then, the substrate insulator layer 302 is formed on the lower light-shielding film 301. the insulator layers (for example, the silicon oxide film, an oxidation silicon nitride film, a silicon nitride film, etc.) in which the substrate insulator layer 302 contains silicon — LPCVD — it forms in law, a plasma-CVD method, or a spatter. And the amorphous semiconductor film (not shown) is formed on the substrate insulator layer 302. Although there

is especially no limitation as amorphous semiconductor film, it is good to form with the silicon film or a silicon germanium ($\text{Si}_x\text{Ge}_{1-x}$: $0 < x < 1$, typically $x = 0.001-0.05$) alloy. In addition, the amorphous silicon film is formed in 65nm of thickness here.

[0069] Subsequently, the amorphous silicon film is crystallized. Heat-treatment of 24 hours is performed at 600 degrees C using a furnace, and the crystalline substance silicon film (not shown) is formed. In addition, although the silicon oxide film is formed in a silicon film front face in this crystallization processing, since it is the very thin film removable by etching etc., it is satisfactory.

[0070] Subsequently, after removing the oxide film formed in the front face of the crystalline substance silicon film, before forming gate dielectric film 304, heat-treatment for the improvement in membrane of the semi-conductor film is performed. The crystalline substance silicon film is heat-treated at 900-1050 degrees C, and an oxide film is formed in the front face of the crystalline substance semi-conductor film. This silicon oxide film is removed. What is necessary is just to form the silicon oxide film in the front face by heat-treating the crystalline substance silicon film so that the thickness of the crystalline substance silicon film may finally be set to 30-50nm. Thickness of the crystalline substance silicon film is set to 35nm in this example. Then, it forms in the configuration of a request of the obtained crystalline substance silicon film, and the semi-conductor layer 303 which has a field used as wiring used as the field which includes the channel formation field, source field, and drain field of TFT behind, and one electrode of retention volume is formed.

[0071] Subsequently, gate dielectric film 304 is formed on a semi-conductor layer (drawing 2 (B)). Then, the impurity element (henceforth p mold impurity element) which gives p mold to the semi-conductor layer of the field which serves as the n channel mold TFT through gate dielectric film 304 is added. Boron (B) or a gallium (Ga) can be used for the element and type target which belong to 13 groups of the periodic table typically as a p mold impurity element. This process is performed in order to control the threshold electrical potential difference of TFT, and it is called channel dope process. p mold impurity element is added by the semi-conductor layer according to this process by the concentration of 1×10^{15} to $1 \times 10^{18} / \text{cm}^3$.

[0072] Subsequently, the impurity element which gives n mold to the semi-conductor layer of the part which forms the mask which consists of a resist and serves as one electrode of the source field of the n channel mold TFT, a drain field, and retention volume (henceforth n mold impurity element) moreover — here — Lynn — using — it adds and n mold impurity range which includes Lynn in high concentration is formed. In this field, Lynn is made to be included by the concentration of 1×10^{20} to $5 \times 10^{21} / \text{cm}^3$.

[0073] Subsequently, wiring 305b (henceforth capacity wiring) used as gate electrode 305a and one electrode of retention volume is formed. As an ingredient of gate electrode 305a and capacity wiring 305b, TaN, Ta, Ti, Mo, W, Cr, Si by which the impurity element was added can be used. In addition, the laminating of the film of these two or more kinds is carried out, and it is good also as a gate electrode.

[0074] Subsequently, n mold impurity element is added in a semi-conductor layer by using a gate electrode as a mask. Here, Lynn is used as an n mold impurity element. The field where this n mold impurity element was added is a low concentration impurity range for making it function as a LDD field of the n channel mold TFT, and is included in this low concentration n mold impurity range by the concentration of 1×10^{16} to $5 \times 10^{18} / \text{cm}^3$.

[0075] Subsequently, the field used as the next n channel mold TFT is covered with a mask, and it adds so that boron may be included in the semi-conductor layer used as the source field of the next p channel mold TFT, or a drain field as a p mold impurity element by the concentration of 3×10^{20} to $5 \times 10^{21} / \text{cm}^3$ (not shown).

[0076] Next, a silicon nitride film, the silicon oxide film, or the nitriding silicon oxide film is formed by 50-500nm of thickness by the plasma-CVD method as the 1st interlayer insulation film 306.

[0077] Then, heat-treatment for activating the impurity element added by each semi-conductor layer is performed. You may carry out by using together the approach using a furnace as the approach of heat-treatment, the approach by laser beam exposure, the lamp annealing method, or these. It is activated at 550-1000 degrees C in an inert gas ambient atmosphere.

[0078] Subsequently, hydrogenation which carries out termination of the dangling bond in a semi-conductor layer by the hydrogen excited thermally is performed. In the ambient atmosphere containing hydrogen, heat-treatment

of 1 hour is performed at 410 degrees C. As a means of other hydrogenation, the plasma hydrogen treating using the hydrogen excited by the plasma may be performed.

[0079] Subsequently, the 2nd interlayer insulation film 307 is formed by 500–1000nm of thickness. As the 2nd interlayer insulation film 307, inorganic insulator layers, such as an acrylic, polyimide, a polyamide, organic resin film called BCB (benz-cyclo-butene), an oxidation silicon nitride film, or nitriding silicon oxide film, may be used. In addition, in this example, an oxidation silicon nitride film is formed by 900nm of thickness, and flattening is performed by the CMP method (drawing 2 (C)).

[0080] Then, the 1st contact hole which reaches the semi-conductor layer 303 is formed, and the wiring 308 which connects each TFT electrically is formed. What is necessary is just to consider as the laminated structure which forms in 300–500nm of thickness the electric conduction film which uses aluminum as a principal component, after forming in 50–100nm of thickness the electric conduction film which uses titanium as a principal component as an ingredient of wiring 308. However, in case a pixel electrode is touched, it is necessary to use the ingredient which does not cause electric corrosion for the maximum upper layer which touches a pixel electrode.

[0081] Subsequently, the 3rd interlayer insulation film 309 is formed. The 3rd interlayer insulation film 309 is formed in 600nm of thickness using an oxidation silicon nitride film (drawing 3 (A)).

[0082] Subsequently, in the field which is mostly in agreement with opening (field which meant controlling a display), the interlayer insulation film, the gate dielectric film, and the substrate insulator layer which were formed at the process till then are removed, and a lower light-shielding film is exposed. In addition, the field (window) where gate dielectric film and an interlayer insulation film were removed is formed in the range larger than the field (opening) which light actually penetrates.

[0083] Subsequently, the up light-shielding film 311 is formed. As an up light-shielding film, light is not penetrated but the electric conduction film which uses aluminum as a principal component is formed by 100–200nm of thickness here as film which has conductivity. In addition, before forming an up light-shielding film, since the ratio (aspect ratio) of a window of the depth and width of face is small, it can form the electric conduction film with a good coverage also by the spatter. An up light-shielding film is formed so that it may become this potential in contact with a lower light-shielding film. In addition, although not illustrated, wiring with which touch-down potential is given is connected to an up light-shielding film and a lower light-shielding film.

[0084] Subsequently, the up light-shielding film for forming the 2nd contact hole for making it flow through removal, drain electrode, and pixel electrode of the lower light-shielding film formed in the base of a window and an up light-shielding film is removed. Both of the processes etch by using as a mask the pattern formed by the resist. In addition, since the height of the field to etch differs and the laminated structures of the film to remove also differ, in order to make a process simple, a removal process is divided and is performed. However, which process may become first (drawing 14).

[0085] Then, after forming the insulator layer 312 which consists of a silicon nitride film, an oxidation silicon nitride film, or nitriding silicon oxide film by the plasma-CVD method on the up light-shielding film 311, flattening of the window is carried out in organic-compound-insulator 313 grades, such as an acrylic, (drawing 3 (B)).

[0086] In addition, a window may be filled using the photoresist film colored R, G, and B, and organic resin film, such as an acrylic, may be formed after that. By using a coloring layer for flattening of a window, the problem about the color gap produced when the coloring layer was prepared in the opposite substrate side is solvable.

[0087] Then, after forming the 4th interlayer insulation film 314 which consists of a silicon nitride film, an oxidation silicon nitride film, or nitriding silicon oxide film, removing a part of insulator layer which has filled the contact hole and exposing a drain electrode by the spatter, the pixel electrode 315 is formed. At this time, it is important to remove an insulator layer so that the pixel electrode 315 may not touch the up light-shielding film 311. In addition, since the liquid crystal display of a transparency mold is produced in this example, the ingredient which forms a pixel electrode is formed by 100nm of thickness by the spatter using the ITO film (compound of indium oxide and the tin oxide) of translucency (drawing 4 , drawing 15). In addition, if the pixel electrode which plated Ag instead of the ITO film into the metal membrane, for example, aluminum, and the conductive ingredient

of protection-from-light nature is formed, it can consider as the display of a reflective mold. Moreover, you may use as a reflecting plate as it is, without removing the up light-shielding film formed in the window base. In this case, liquid crystal is controlled by the transparent pixel electrode and transparent counterelectrode which are formed on the flattening film.

[0088] TFT320 which consists of the substrate insulator layer covered with the lower light-shielding film and the up light-shielding film, a semi-conductor layer, gate dielectric film, and a gate electrode on a substrate according to the above processes, It has the retention volume 321 which consists of capacity wiring formed in the same layer as the insulator layer of the semi-conductor layer used as one electrode, and the same layer as the gate dielectric film used as a dielectric, and a gate electrode. The active-matrix substrate comparatively (numerical aperture) exceeding 50% of the field which the light to pixel area penetrates is producible.

[0089] Moreover, after sticking the opposite substrate and active-matrix substrate with which the orientation film which carries out orientation of the liquid crystal layer to the active-matrix substrate obtained by doing in this way was formed, and a counterelectrode and the orientation film were formed using the well-known cel **** technique, an active matrix liquid crystal display can be completed by pouring in liquid crystal.

[0090] (Example 2) By this example, by forming the up light-shielding film of two or more sheets explains how to form retention volume along with the wall surface of the field (window) where some of gate dielectric film and interlayer insulation films were removed at least.

[0091] It changes into the condition that the lower light-shielding film of the base of the window shown in drawing 3 (A) was exposed according to the production process shown in the example 1 (drawing 5 (A)).

[0092] Subsequently, the 1st light-shielding film 401 of the upper part is formed. As the 1st light-shielding film 401 of the upper part, the electric conduction film (aluminum, chromium, electric conduction film that uses as a principal component the element chosen from titanium) is formed by 100-200nm of thickness. Then, the 2nd contact hole which reaches wiring 308 is formed in the 1st light-shielding film 401 of the upper part, and the 3rd interlayer insulation film 309. In addition, the 1st contact hole is a contact hole for connecting wiring and a semi-conductor layer.

[0093] Subsequently, the 1st insulator layer 402 which consists of an oxidation silicon nitride film, nitriding silicon oxide film, or a silicon nitride film is formed by a plasma-CVD method etc. on the 1st light-shielding film 401 of the upper part.

[0094] Subsequently, after removing a part of 1st insulator layer which has filled the 2nd contact hole and exposing the 1st light-shielding film 401 of the upper part, the 2nd light-shielding film 403 of the upper part is formed on the 1st insulator layer 402. In addition, the laminating of the electric conduction film of the quality of the material which contacts the ITO film used as a pixel electrode, and does not cause electric corrosion is carried out, and the 2nd light-shielding film 403 of the upper part forms it, in order to connect with a pixel electrode. In addition, in this example, after forming the electric conduction film which uses aluminum as a principal component, it considers as the structure where the laminating of the electric conduction film which uses a tungsten as a principal component was carried out to the side which touches a pixel electrode. In addition, the thickness of the 2nd light-shielding film 403 of the upper part may be 100-200nm. Then, the 2nd insulator layer 404 is formed like the 1st insulator layer on the 2nd light-shielding film 403 of the upper part.

[0095] Subsequently, the 3rd light-shielding film 405 of the upper part is formed on the 2nd insulator layer 404. In addition, the 3rd light-shielding film of the upper part is electrically connected to the lower light-shielding film 301 or the 1st light-shielding film 401 of the upper part so that it may become the lower light-shielding film 301 and the 1st light-shielding film 401 of the upper part, and this potential (it considers as touch-down potential in this example). In addition, what is necessary is just to connect wiring so that it may be made to connect in fields other than a pixel without a problem which lowers a numerical aperture for connection and may become touch-down potential.

[0096] Subsequently, the 3rd contact hole formation for taking a flow with the pixel electrode and the 2nd light-shielding film 403 of the upper part which are formed behind, and removal of the lower light-shielding film 301 at the base of a window, the 1st light-shielding film 401 of the upper part, the 2nd light-shielding film 403 of the

upper part, and the 3rd light-shielding film 405 of the upper part are performed.

[0097] Subsequently, the 4th interlayer insulation film 406 is formed on the 3rd light-shielding film 405 of the upper part. In addition, what is necessary is to form the 4th interlayer insulation film 406 as well as the 1st insulator layer 402 and the 2nd insulator layer 404 by the plasma-CVD method, and just to use the insulator layer chosen from a silicon nitride film, an oxidation silicon nitride film, the nitriding silicon oxide film, etc.

[0098] Subsequently, flattening of a window is performed. What is necessary is just to perform the flattening film 407 using organic compound insulators, such as an acrylic, like an example 1. Moreover, as shown also in the example 1, after filling a window using the photoresist film colored R, G, and B, organic resin film, such as an acrylic, may be performed for flattening.

[0099] Then, by the spatter, the 5th interlayer insulation film 408 which consists of a silicon nitride film, an oxidation silicon nitride film, or nitriding silicon oxide film is formed in the whole surface, a part of insulator layer which has filled the 3rd contact hole is removed, and the 2nd light-shielding film 403 of the upper part is exposed. And the pixel electrode 409 is formed so that the 2nd light-shielding film 403 of the upper part may not be touched. The ingredient which forms the pixel electrode 409 is formed by 100nm of thickness by the spatter using the ITO film (compound of indium oxide and the tin oxide) of translucency.

[0100] The 2nd retention volume 503 which considers the 1st retention volume 502 which considers the 1st light-shielding film 401 of the upper part as one capacity wiring, uses the 1st insulator layer 402 as a dielectric, and considers the 2nd light-shielding film 403 of the upper part as another capacity wiring according to the above process, and the 2nd light-shielding film 403 of the upper part as one capacity wiring, uses the 2nd insulator layer 404 as a dielectric, and considers the 3rd light-shielding film 405 of the upper part as another capacity wiring is formed along the side face of a window. In addition, although capacity sufficient with the 1st retention volume and the 2nd retention volume can be obtained, the retention volume which consists of an insulator layer of a semiconductor layer and the same layer as gate dielectric film and capacity wiring of the same layer as a gate electrode like an example 1 may be formed collectively.

[0101] In order to enlarge capacity of a retention volume component further, after removing a part of lower light-shielding film formed in the base of a window, the exposed substrate may be shaved and a retention volume component may be made to extend to the interior of a substrate.

[0102] Moreover, wiring 308, the 2nd light-shielding film 403 of the upper part and the 2nd light-shielding film 403 of the upper part, and the pixel electrode 409 can be connected, finally the pixel electrode 409 and wiring 308 can be connected electrically, and TFT501 can be used as the switching element of a pixel. Moreover, since the aspect ratio of a contact hole can be reduced by considering wiring and a pixel electrode as two steps of connection through an up light-shielding film like this example, processing is easy and good coverage can be further obtained also by the spatter in the case of membrane formation. Moreover, as compared with the case where a contact hole is thin and long, contact resistance can be made low. Moreover, if the location of the contact hole of a pixel electrode (ITO) and the 2nd up light-shielding film is shifted and formed from the location of the contact hole of the 2nd up light-shielding film and wiring, protection-from-light nature can improve and the problem which the leakage current by optical pumping generates can also be solved.

[0103] As mentioned above, since the retention volume which can cover TFT completely by forming two or more up light-shielding film layers so that TFT may be inserted in, and has sufficient capacity can be formed along the side face of a window, a numerical aperture can be gathered further.

[0104] (Example 3) This example explains an example of the active matrix liquid crystal display produced using the active-matrix substrate produced using examples 1 or 2.

[0105] In drawing 7, a active-matrix substrate consists of the pixel section and the drive circuit which were formed on the substrate, and other digital disposal circuits. The drive circuit which TFT (it is also called Pixel TFT) and retention volume are formed in the pixel section, and is formed around the pixel section is constituted on the basis of a CMOS circuit.

[0106] From the drive circuit, the gate line and the source line are extended and formed in the pixel section, and have connected with Pixel TFT. Moreover, it is used for FPC (flexible printed wiring board) having connected with

an external input terminal, and inputting a picture signal etc. In addition, it has pasted up firmly with reinforcement resin and FPC is connected to each drive circuit with connection wiring. Moreover, the counterelectrode is formed although not illustrated in an opposite substrate.

[0107] The active matrix liquid crystal display formed using this invention can perform a quality display, without being able to suppress generating of the optical leakage current by the stray light, and changing the potential of a pixel electrode, since it is formed so that a light-shielding film may insert in on TFT.

[0108] (Example 4) The pixel of other structures using this invention is explained using drawing 13 .

[0109] Even the 2nd interlayer insulation film 16 forms according to the process of an example 1. Then, a slot is formed in the boundary line of the field and TFT which light penetrates at the process which forms the 1st contact hole semi-conductor layer carried out, and the wiring 50 which connects each TFT electrically is formed. Wiring is continuously formed so that it may be filled up with a slot from on the 2nd interlayer insulation film.

[0110] Then, the 3rd interlayer insulation film 18 is formed and the up light-shielding film 19 is formed. Then, the 2nd contact hole for connecting wiring with a pixel electrode is formed, and the 4th interlayer insulation film 20 is formed. After removing a part of insulator layer buried with extent to which a pixel electrode does not touch a light-shielding film in the 2nd contact hole, the pixel electrode 21 is formed.

[0111] Moreover, other examples are shown in drawing 13 (B). The contact hole which even the 2nd interlayer insulation film 16 forms and continues according to the process of an example 1, and reaches a semi-conductor layer is formed, the substrate insulator layer 11 of a field a little larger than opening, gate dielectric film 13, the 1st interlayer insulation film 15, and the 2nd interlayer insulation film 16 are removed, and a window is formed.

[0112] Then, each wiring which connects TFT electrically is formed. Wiring is continuously formed along with the wall surface of a window from on the 2nd interlayer insulation film 16. After removing wiring formed in the base of a window, the 3rd interlayer insulation film 18 is formed, and a light-shielding film 19 is formed continuously. Subsequently, after forming the 4th interlayer insulation film 20, the flattening film 30 of a window is formed and the 5th interlayer insulation film 31 is formed. And after removing a part of insulator layer buried with extent to which a pixel electrode does not touch a light-shielding film in the 2nd contact hole, the pixel electrode 32 is formed.

[0113] As mentioned above, even if it uses wiring and a light-shielding film, it is possible to shade the semi-conductor layer of TFT.

[0114] (Example 5) This example explains the process which forms a crystalline substance semi-conductor layer.

[0115] The lower light-shielding film 1201 and the substrate insulator layer 1202 are formed on a substrate 1200. Then, the amorphous silicon film 1203 is formed as amorphous semiconductor film on the substrate insulator layer 1202. Then, a mask 1204 is formed on the amorphous silicon film 1203, the metallic element (henceforth a catalyst element) which has the operation which promotes crystallization on the amorphous silicon film exposed from opening of a mask is added, and the catalyst content layer 1205 is formed. It is metallic elements which can be used as a catalyst element, such as nickel, Fe, Co, Ru, Rh, Pd, Os, Pt, and Au. In this example, nickel (nickel) is used as a catalyst element (drawing 8 (A)).

[0116] Then, in nitrogen-gas-atmosphere mind, heat-treatment of 12 hours (4 – 12 hours) is performed at 600 degrees C (500–700 degrees C), and the crystalline substance silicon film 1206 is formed (drawing 8 (B)). In addition, in order to reduce the hydrogen contained in the amorphous silicon film as pretreatment which performs heat-treatment for crystallization, heat-treatment of 1 hour may be performed at 450 degrees C. Furthermore, after performing heat-treatment for crystallization, a laser beam may be irradiated in order to raise the crystallinity of the crystalline substance silicon film (drawing 8 (C)).

[0117] Subsequently, heat-treatment for reducing the concentration of the catalyst element contained in the crystalline substance silicon film is performed. It is because it is thought that it segregates to the grain boundary in the silicon film, this segregation serves as a recess path (leak pass) of a feeble current, and the catalyst element causes a sudden increment in the OFF state current (current in case TFT is in an OFF state).

[0118] First, a mask 1208 is formed on the crystalline substance silicon film, and the element (typically Lynn) which belongs to the crystalline substance silicon film at 15 groups of a periodic table is added. The gettering site

1209 which includes Lynn by the concentration of 1×10^{19} to 1×10^{20} /cm³ is formed in the crystalline substance silicon film exposed from mask opening. In addition, in this specification, the field where the element belonging to 15 groups of a periodic table is added, and a catalyst element moves by heat-treatment is called gettering site. [0119] Subsequently, heat-treatment of 4 – 24 hours is performed at 450–650 degrees C in nitrogen-gas-atmosphere. Since the catalyst element in the crystalline substance silicon film moves to a gettering site, three or less 1×10^{16} /cm can be made to reduce preferably the catalyst element concentration in the crystalline substance silicon film three or less 1×10^{17} /cm by this heat-treatment.

[0120] The crystalline substance silicon film obtained using the catalyst element as mentioned above has the crystal structure located in a line with the cylindrical or directivity of specification [a column-like crystal], and its crystallinity is very good. By using such a semi-conductor layer, TFT with a sufficient property is producible. In addition, this example can be used combining examples 1 and 2.

[0121] (Example 6) This example explains the process which forms a crystalline substance semi-conductor layer.

[0122] On a substrate 1100, the lower light-shielding film 1101 and the substrate insulator layer 1102 are formed. Then, the amorphous silicon film 1103 is formed by 200nm of thickness on the substrate insulator layer 1102. Subsequently, a catalyst element is added on the amorphous silicon film. In this example, the water solution (nickel acetate water solution) which contains 10 ppm nickel by weight conversion is applied with a spin coat method, using nickel as a catalyst element, and the catalyst element content layer 1104 is formed. In addition, it is also possible to use a spatter and vacuum deposition and to add a catalyst element besides a spin coat method, (drawing 9 (A)).

[0123] Subsequently, heat-treatment of about 1 hour is performed at 400–500 degrees C before heat-treatment for crystallization, and the hydrogen contained in the amorphous silicon film is desorbed. Then, in order to perform heat-treatment for crystallization, heat-treatment of 4 – 12 hours is performed at 500–650 degrees C, and the crystalline substance silicon film 1105 is formed (drawing 9 (B)). Then, further, in order to raise crystallinity, a laser beam may be irradiated (drawing 9 (C)).

[0124] Subsequently, the process which reduces the concentration of the catalyst element which remains on the crystalline substance silicon film 1105 is performed. It is thought that the catalyst element is contained in the crystalline substance silicon film 1105 by three or more 1×10^{19} /cm concentration. Although it was possible to have produced TFT using the crystalline substance [that the catalyst element has remained] silicon film 1105, the catalyst element segregated to the defect of a semi-conductor layer, and there was a problem that an OFF state current value will rise suddenly. Then, a catalyst element is removed from the crystalline substance silicon film 1105, and heat-treatment aiming at decreasing even to three or less 1×10^{16} /cm concentration preferably is performed three or less 1×10^{17} /cm.

[0125] The barrier layer 1106 is formed in the front face of the crystalline substance silicon film 1105. In case the barrier layer 1106 removes the gettering site 1107 behind prepared on the barrier layer 1106 by etching, it is a layer provided so that the crystalline substance silicon film 1105 may not be etched.

[0126] The barrier layer 1106 is made into about 1–10nm in thickness, and should just use as a barrier layer the chemical oxide formed by processing the crystalline substance silicon film with ozone water simple. Even if it is as other examples with the water solution which mixed hydrogen peroxide solution with the sulfuric acid, the hydrochloric acid, the nitric acid, etc., chemical oxide can be formed similarly. Moreover, it may oxidize by performing UV irradiation in the plasma treatment in the inside of an oxidizing atmosphere, or an oxygen content ambient atmosphere, and generating ozone as an example of other barrier layers, and a barrier layer may be formed. Furthermore, after heating at about 200–350 degrees C, using clean oven as another example, a thin oxide film is formed and it is good also as a barrier layer.

[0127] Subsequently, the gettering site 1107 is formed by the spatter on the barrier layer 1106. As a gettering site 1107, the amorphous silicon film is formed in the semi-conductor film and representation target which contain rare gas by three or more 1×10^{20} /cm concentration by the thickness of 25–250nm. In order for etching to remove the gettering site 1107 after gettering process termination, it is desirable to consider as the film with a low consistency with the crystalline substance silicon film 1105, so that the selection ratio of etching may

become large.

[0128] It sets [Ar] a membrane formation pressure to 0.2–1.0Pa for 50sccm(s) and membrane formation power, setting 3kW and substrate temperature as 150 degrees C, and the gettering site 1107 forms membranes by the spatter. Thus, the gettering site 1107 which contains a rare-gas element by the concentration of 1×10^{19} to 1×10^{22} /cm³ can be formed. In addition, in the semi-conductor film, since a rare-gas element is inactive, it cannot have a bad influence on the crystalline substance silicon film 1105, and can perform gettering.

[0129] Subsequently, heat-treatment for finishing gettering certainly is performed. the heating art for which heat-treatment uses a furnace, and RTA which uses a lamp or the heated gas for a heat source — what is necessary is just to carry out by law What is necessary is just to carry out heat-treatment of 0.5 – 12 hours at 450–600 degrees C in nitrogen-gas-atmosphere mind, in using a furnace. When using the RTA method, the semi-conductor film should just be momentarily heated to about 600–1000 degrees C.

[0130] By such heat-treatment, the catalyst element which remains on the crystalline substance silicon film 1105 can move to the gettering site 1107, and the concentration of the catalyst element of the crystalline substance silicon film 1105 can be preferably reduced in three or less 1×10^{16} /cm³ or less 1×10^{17} /cm³. In addition, the gettering site 1107 is not crystallized in the case of heat-treatment for gettering. This is considered because it remains to the gettering site, without being emitted also while a rare-gas element heat-treats.

[0131] If gettering processing is completed, etching will remove the gettering site 1107. Etching can use the wet etching by alkali solutions, such as dry etching which does not use the plasma by ClF₃, or a water solution containing a hydrazine or tetraethylammonium hydroxide (CH₃)₄NOH. In addition, in this etching process, the barrier layer 1106 functions as an etching stopper which prevents the film from being crystalline substance semi-conductor etched [1105]. Moreover, what is necessary is just to remove the barrier layer 1106 by fluoric acid etc., if removal by etching of the gettering site 1107 finishes.

[0132] The crystalline substance silicon film 1105 obtained using the catalyst element as mentioned above has the crystal structure located in a line with the cylindrical or directivity of specification [a column-like crystal], and its crystallinity is very good. Since the catalyst element concentration in the crystalline substance silicon film can furthermore fully be reduced, TFT with a sufficient property is producible by using such a semi-conductor layer. In addition, this example can be used combining examples 1 and 2.

[0133] (Example 7) By forming the film (it being called the organic compound layer) and cathode containing the organic compound with which luminescence is obtained by adding electric field on the pixel electrode of the TFT substrate using this invention explains how to form luminescence equipment.

[0134] According to an example 1, TFT (TFT for current control) for controlling the current which flows to a light emitting device (an anode plate, an organic compound layer, laminating that consists of cathode) is formed on a substrate, a window 310 is formed, the up light-shielding film 311 and an insulator layer 312 are formed, and flattening of a window 310 is continuously performed using an organic compound insulator 313. In addition, in this example, TFT for current control should be just adapted in the p channel mold TFT.

[0135] Subsequently, after carrying out flattening of the level difference of an insulator layer 312 and an organic compound insulator 313 with the 4th interlayer insulation film 314, the pixel electrode (it is also called an anode plate) 700 is formed, and it forms to the condition shown in drawing 3 (B). In addition, since flattening of the level difference of an insulator layer 312 and an organic compound insulator 313 is not necessarily required, an operation person should just carry out suitably if needed. Subsequently; if the pixel electrode (anode plate) 700 is formed, the bank 701 which becomes a wrap sake from the organic resin film about the edge of an anode plate 700 will be formed. Since an organic compound layer is not formed in the edge of an anode plate by forming the organic resin film, electric-field concentration of an organic compound layer can be prevented. Subsequently, the organic resin film currently formed in the field which light penetrates is removed, an anode plate 700 is exposed, an insulator layer 702 is formed on an anode plate 700, and the organic compound layer 703 and cathode 704 are formed on an insulator layer.

[0136] An insulator layer 702 should just form organic resin film, such as polyimide, a polyamide, and polyimidoamide, by 1–5nm of thickness using a spin coat method, vacuum deposition, or a spatter.

[0137] The thickness as an organic substance combination layer 703 has [an organic compound 703 / that what is necessary is to carry out a laminating and just to form as a hole-injection layer combining two or more layers called the electron hole transportation layer, the electron hole blocking layer, the electronic transportation layer, electron injection layer, and buffer layer other than a luminous layer] desirable about 10–400nm.

[0138] Cathode 704 is formed with vacuum deposition after organic compound layer 703 formation. The film which formed the element belonging to one group of a periodic table or two groups other than MgAg or an aluminum-Li alloy (alloy of aluminum and a lithium) and aluminum with vapor codeposition as an ingredient used as cathode 704 may be used. In addition, the thickness of cathode 704 has desirable about 80–200nm. Thus, luminescence equipment as shown in drawing 16 (A) is producible.

[0139] In addition, after forming an insulator layer 312 according to an example 1, flattening of a window 310 cannot be performed, but as shown in drawing 16 (B), an anode plate 1700, an insulator layer 1701, the organic compound layer 1702, and cathode 1703 can also be formed in the interior of a window. Since it is not necessary to form the bank for preventing forming an organic compound layer in the edge of an anode plate by doing in this way, a manufacturing cost can be reduced.

[0140] Moreover, since the luminescence field of a light emitting device spreads by digging the glass substrate of a field equivalent to opening formed in the window 310, and making thickness of a glass substrate thinner than other fields, it is also possible to raise the brightness as luminescence equipment.

[0141] Thus, the adaptation range of this invention can be wide, and can be adapted besides a liquid crystal display. In addition, it is possible, although it is adapted combining the operation gestalten 1–3, examples 1–2, and 4, 5 and 6 in this example and luminescence equipment is produced.

[0142] (Example 8) the active matrix liquid crystal display (a liquid crystal display or EL display) formed by carrying out this invention — a display — incorporating — high definition — high — the electric appliance in which a brightness display is possible is realizable.

[0143] As such an electric appliance, a projector, a video camera, a digital camera, a head mount display (goggles mold display), a personal computer, Personal Digital Assistants (a mobile computer, a cellular phone, or digital book), etc. are mentioned. Those examples are shown in drawing 10 , drawing 11 , and drawing 12 .

[0144] Drawing 10 (A) is a front mold projector, and contains a projection device 2601 and screen 2602 grade.

[0145] Drawing 10 (B) is a rear mold projector, and contains a body 2701, a projection device 2702, a mirror 2703, and screen 2704 grade.

[0146] In addition, drawing 10 (C) is drawing having shown an example of the structure of the projection devices 2601 and 2702 in drawing 10 (A) and drawing 10 (B). Projection devices 2601 and 2702 consist of the light source optical system 2801, mirrors 2802, 2804–2806, a dichroic mirror 2803, prism 2807, a liquid crystal display 2808, a phase contrast plate 2809, and an incident light study system 2810. The incident light study system 2810 consists of optical system containing a projector lens. Although this example showed the example of a 3 plate type, it may not be limited especially, for example, may be a veneer type. Moreover, an operation person may prepare suitably the optical system of an optical lens, the film which has a polarization function, the film for adjusting phase contrast, IR film, etc., etc. in the optical path shown by the arrow head in drawing 10 (C).

[0147] Moreover, drawing 10 (D) is drawing having shown an example of the structure of the light source optical system 2801 in drawing 10 (C). The light source optical system 2801 is constituted from this example by a reflector 2811, the light source 2812, the lens arrays 2813 and 2814, the polarization sensing element 2815, and the condenser lens 2816. In addition, the light source optical system shown in drawing 10 (D) is especially an example, and is not limited. For example, an operation person may prepare suitably the optical system of an optical lens, the film which has a polarization function, the film which adjusts phase contrast, IR film, etc. in light source optical system.

[0148] Drawing 11 (A) is a personal computer and contains a body 2001, the image input section 2002, a display 2003, and keyboard 2004 grade.

[0149] Drawing 11 (B) is a video camera and contains a body 2101, a display 2102, the voice input section 2103, the actuation switch 2104, a dc-battery 2105, and television section 2106 grade.

[0150] Drawing 11 (C) is a mobile computer (Mobile computer), and contains a body 2201, the camera section 2202, the television section 2203, the actuation switch 2204, and display 2205 grade.

[0151] Drawing 11 (D) is a goggles mold display, and contains a body 2301, a display 2302, and arm section 2303 grade.

[0152] Drawing 11 (E) is a player using the record medium (it is hereafter called a record medium) which recorded the program, and contains a body 2401, a display 2402, the loudspeaker section 2403, a record medium 2404, and actuation switch 2405 grade. In addition, this player can use music appreciation, movie appreciation, a game, and the Internet, using DVD (Digital Versatile Disc), CD, etc. as a record medium.

[0153] Drawing 11 (F) is a digital camera and contains a body 2501, a display 2502, an eye contacting part 2503, the actuation switch 2504, the television section (not shown), etc.

[0154] Drawing 12 (A) is a cellular phone, 3001 is a panel for a display and 3002 is a panel for actuation. The panel 3001 for a display and the panel 3002 for actuation are connected in the connection 3003. The include angle theta of the field in which the display 3004 of the panel 3001 for a display in a connection 3003 is formed, and the field in which the actuation key 3006 of the panel 3002 for actuation is formed is changeable into arbitration. Furthermore, it has the voice output section 3005, the actuation key 3006, an electric power switch 3007, and the voice input section 3008.

[0155] Drawing 12 (B) is pocket books (digital book), and contains a body 3101, displays 3102 and 3103, a storage 3104, the actuation switch 3005, and antenna 3106 grade.

[0156] Drawing 12 (C) is a display and contains a body 3201, susceptor 3202, and display 3203 grade.

[0157] As mentioned above, the applicability of this invention is very wide, and applying to the electric appliance of all fields is possible. Moreover, the electric appliance of this example is realizable combining examples 1-4.

[0158]

[Effect of the Invention] Since TFT can be completely covered by the lower light-shielding film and the up light-shielding film by forming a light-shielding film by using this invention so that TFT may be inserted in, optical leakage current can be controlled. Moreover, sufficient retention volume can be secured, without lowering a numerical aperture.

[0159] using such a protection-from-light technique of TFT — high definition and a high definition — high — being able to realize the possible display of a brightness display and using such a display for the display of an electric appliance — high definition and a high definition — high — the electric appliance in which a brightness display is possible is realizable.

[Translation done.]

* NOTICES *

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.*** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] Drawing showing an example of the semiconductor device produced using this invention.

[Drawing 2] Drawing showing an example of operation of this invention.

[Drawing 3] Drawing showing an example of operation of this invention.

[Drawing 4] Drawing showing an example of operation of this invention.
[Drawing 5] Drawing showing an example of operation of this invention.
[Drawing 6] Drawing showing an example of operation of this invention.
[Drawing 7] Drawing showing an example of operation of this invention.
[Drawing 8] Drawing showing an example of operation of this invention.
[Drawing 9] Drawing showing an example of operation of this invention.
[Drawing 10] Drawing showing an example of an electric appliance.
[Drawing 11] Drawing showing an example of an electric appliance.
[Drawing 12] Drawing showing an example of an electric appliance.
[Drawing 13] Drawing showing an example of operation of this invention.
[Drawing 14] Drawing showing an example of operation of this invention.
[Drawing 15] Drawing showing an example of operation of this invention.
[Drawing 16] Drawing showing an example of operation of this invention.

[Translation done.]